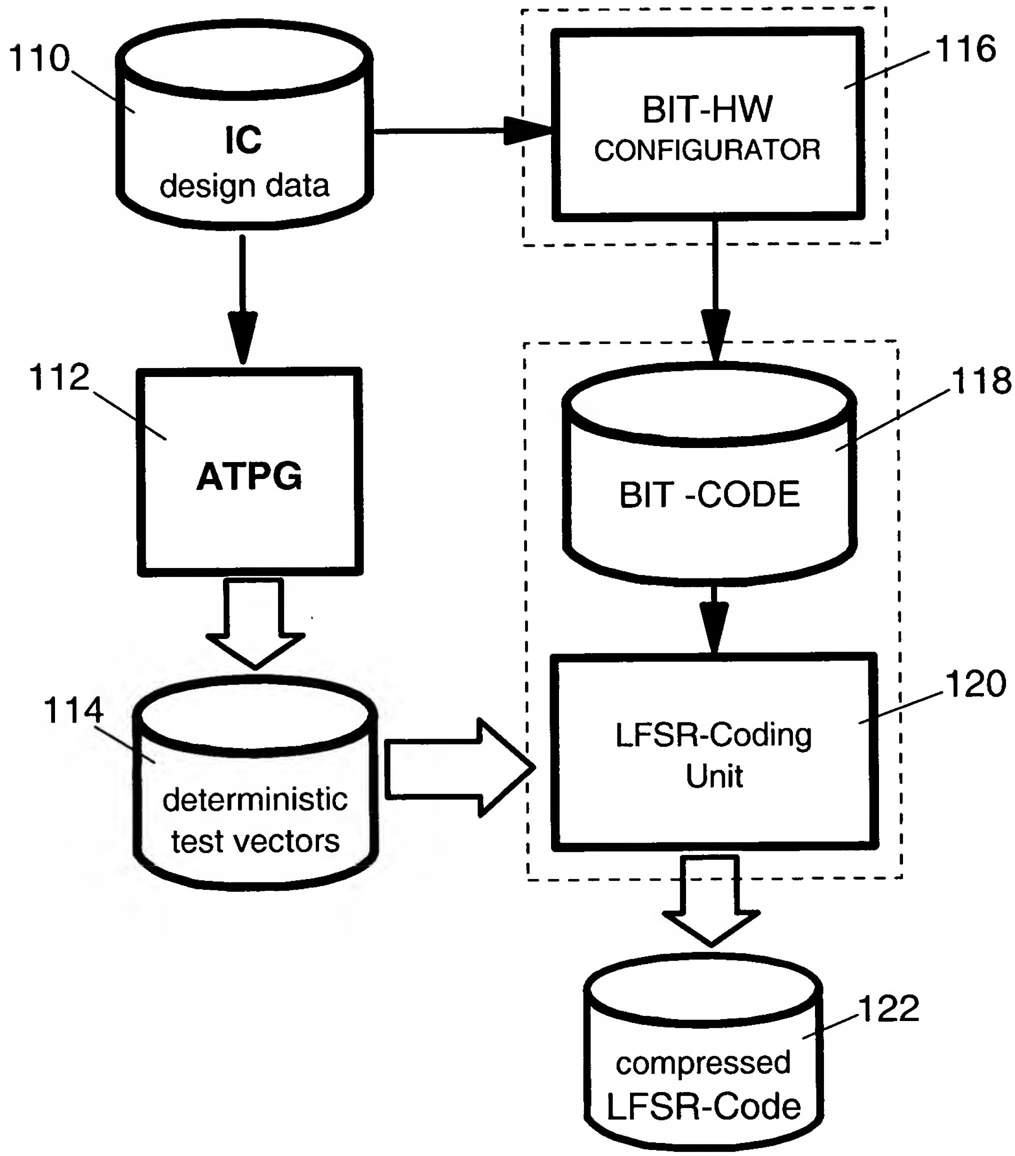

110
IC
design data
116
BIT-HW
CONFIGURATOR
112
ATPG
118
BIT -CODE
114
deterministic
test vectors
120
LFSR-Coding
Unit
122
compressed
LFSR-Code

FIG. 1

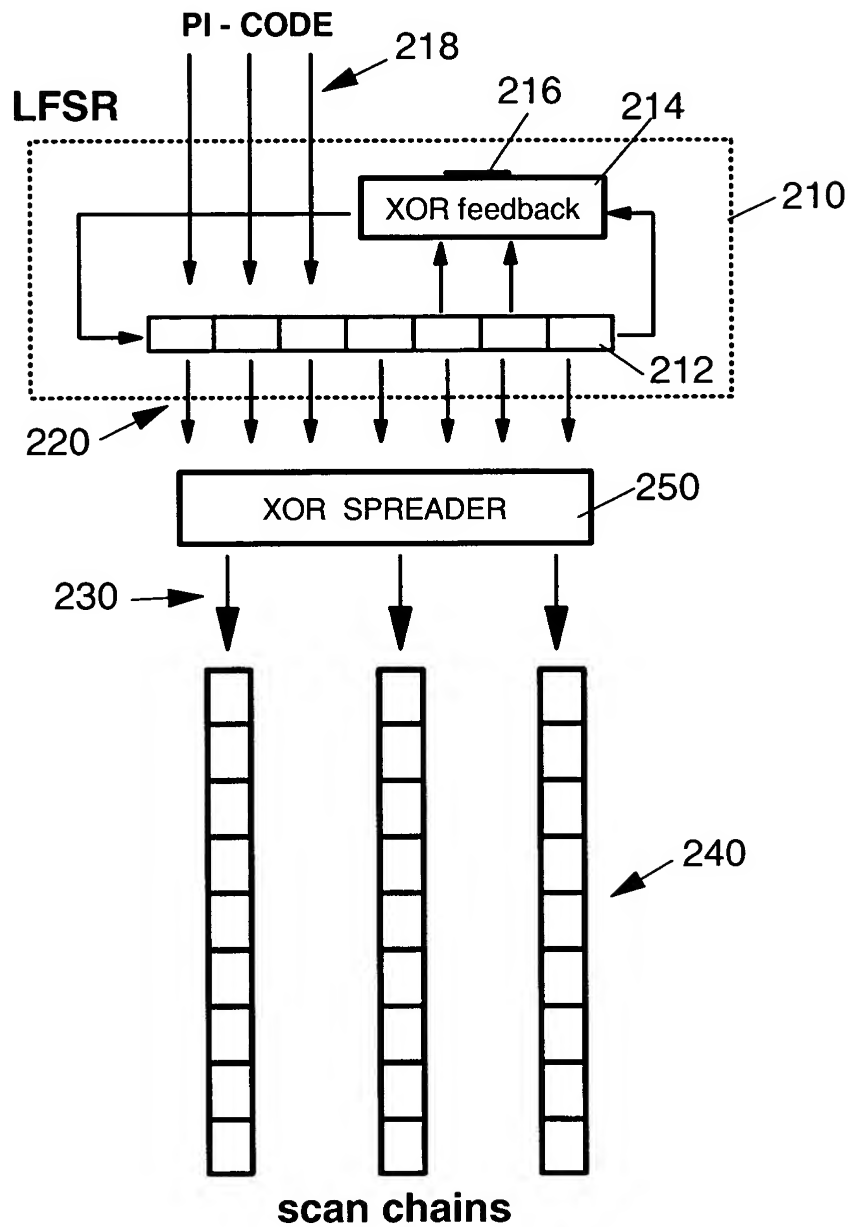

PI - CODE
218
LFSR
216
214
XOR feedback
210
212
220
XOR SPREADER
250
230
240
scan chains

FIG. 2

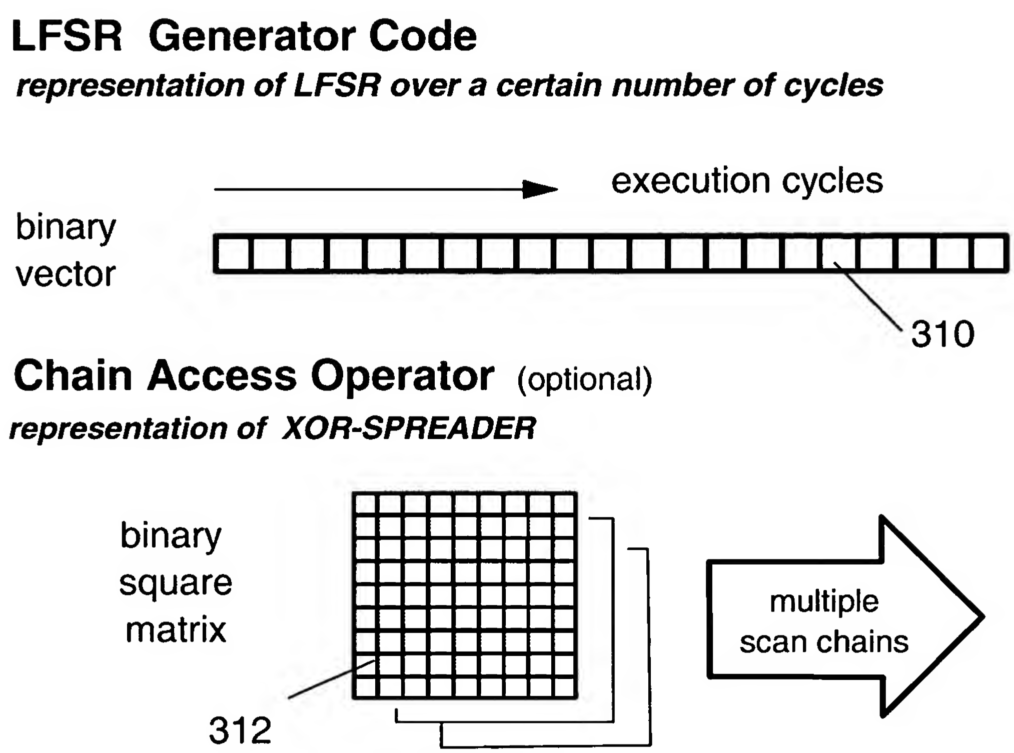

LFSR Generator Code
representation of LFSR over a certain number of cycles
execution cycles
binary
vector
310
Chain Access Operator (optional)
representation of XOR-SPREADER
binary
square
matrix
312
multiple
scan chains

FIG. 3

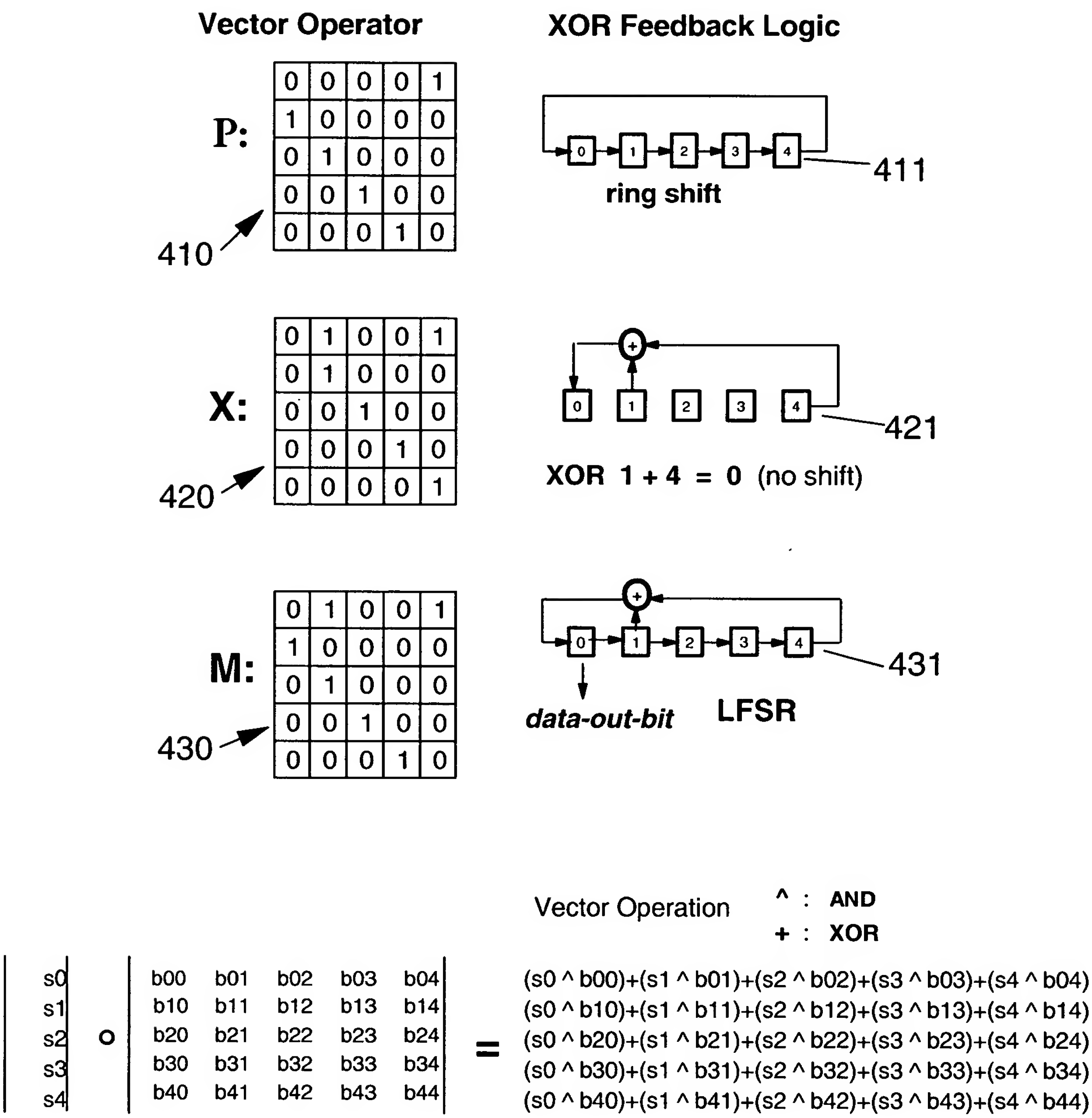
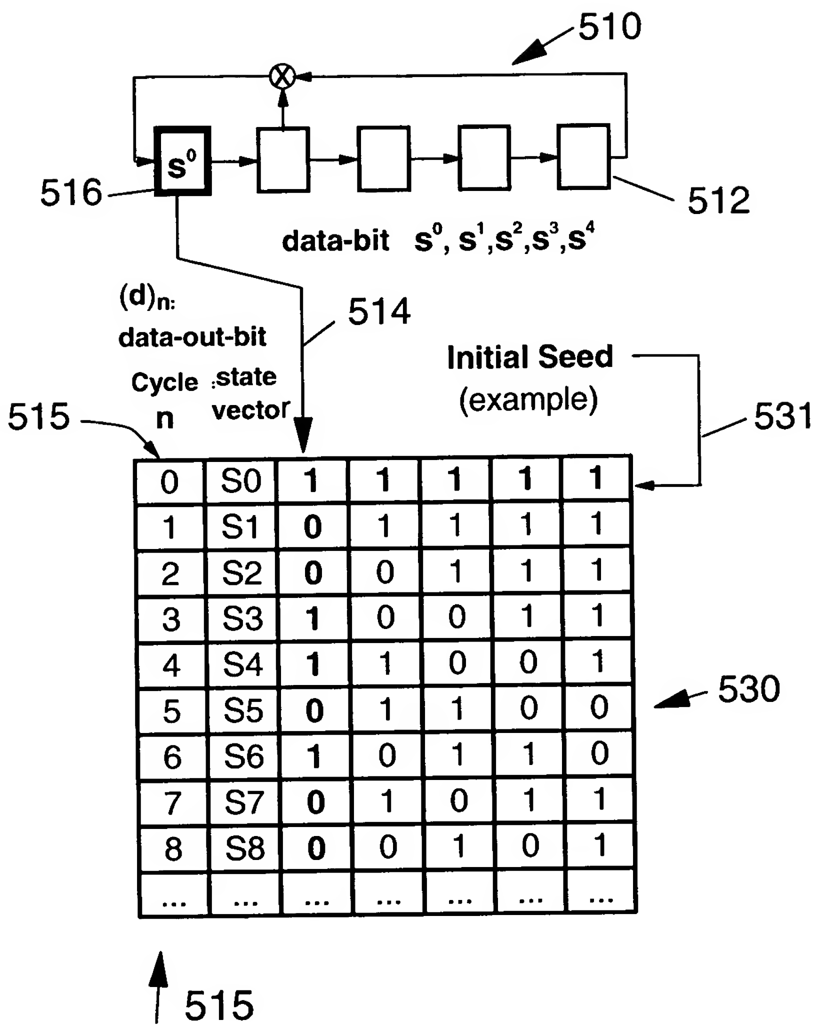

Vector Operator
XOR Feedback Logic
P:
0 0 0 0 1
1 0 0 0 0
0 1 0 0 0
0 0 1 0 0
0 0 0 1 0
410
0 1 2 3 4
ring shift
411
X:
0 1 0 0 1
0 1 0 0 0
0 0 1 0 0
0 0 0 1 0
0 0 0 0 1
420
0 1 2 3 4
421
XOR 1 + 4 = 0 (no shift)
M:
0 1 0 0 1
1 0 0 0 0
0 1 0 0 0
0 0 1 0 0
0 0 0 1 0
430
0 1 2 3 4
431
data-out-bit
LFSR
Vector Operation
^ : AND
+ : XOR
s0 s1 s2 s3 s4
o
b00 b01 b02 b03 b04
b10 b11 b12 b13 b14
b20 b21 b22 b23 b24
b30 b31 b32 b33 b34
b40 b41 b42 b43 b44
=
(s0 ^ b00)+(s1 ^ b01)+(s2 ^ b02)+(s3 ^ b03)+(s4 ^ b04)
(s0 ^ b10)+(s1 ^ b11)+(s2 ^ b12)+(s3 ^ b13)+(s4 ^ b14)
(s0 ^ b20)+(s1 ^ b21)+(s2 ^ b22)+(s3 ^ b23)+(s4 ^ b24)
(s0 ^ b30)+(s1 ^ b31)+(s2 ^ b32)+(s3 ^ b33)+(s4 ^ b34)
(s0 ^ b40)+(s1 ^ b41)+(s2 ^ b42)+(s3 ^ b43)+(s4 ^ b44)

FIG. 4



Cycle n	state vector					
0	S0	**1**	**1**	**1**	**1**	**1**
1	S1	**0**	1	1	1	1
2	S2	**0**	0	1	1	1
3	S3	**1**	0	0	1	1
4	S4	**1**	1	0	0	1
5	S5	**0**	1	1	0	0
6	S6	**1**	0	1	1	0
7	S7	**0**	1	0	1	1
8	S8	**0**	0	1	0	1
...	...	...	...	...	...	...

FIG. 5

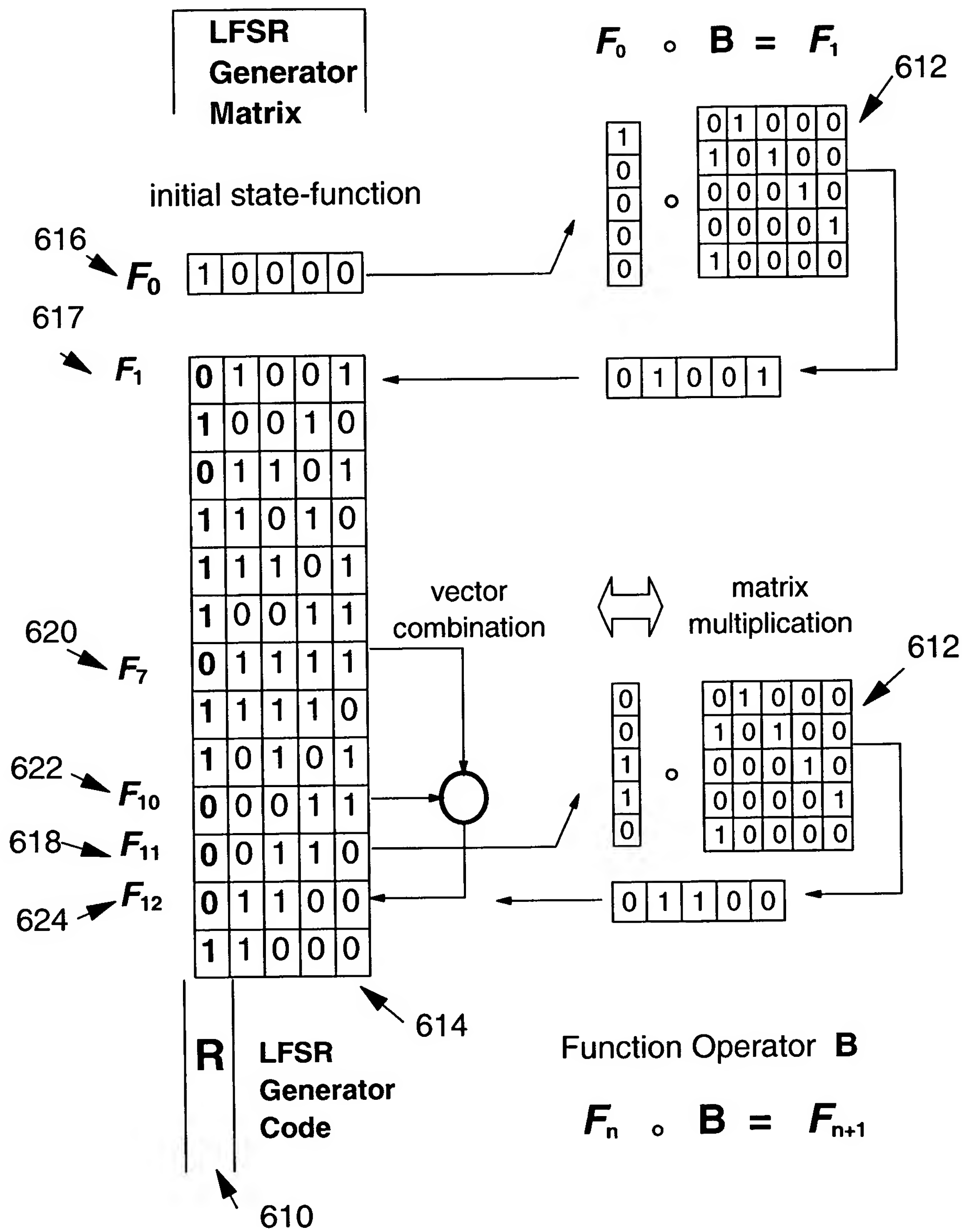

LFSR
Generator
Matrix
initial state-function
616
F_0
1 0 0 0 0
617
F_1
$F_0 \circ B = F_1$
612
1 0 0 0 0
0 1 0 0 0
1 0 1 0 0
0 0 0 1 0
0 0 0 0 1
1 0 0 0 0
0 1 0 0 1
0 1 0 0 1
1 0 0 1 0
0 1 1 0 1
1 1 0 1 0
1 1 1 0 1
1 0 0 1 1
0 1 1 1 1
1 1 1 1 0
1 0 1 0 1
0 0 0 1 1
0 0 1 1 0
0 1 1 0 0
1 1 0 0 0
620
F_7
622
F_{10}
618
F_{11}
624
F_{12}
vector
combination
matrix
multiplication
612
0 0 1 1 0
0 1 0 0 0
1 0 1 0 0
0 0 0 1 0
0 0 0 0 1
1 0 0 0 0
0 1 1 0 0
614
R
LFSR
Generator
Code
610
Function Operator B
$F_n \circ B = F_{n+1}$

FIG. 6

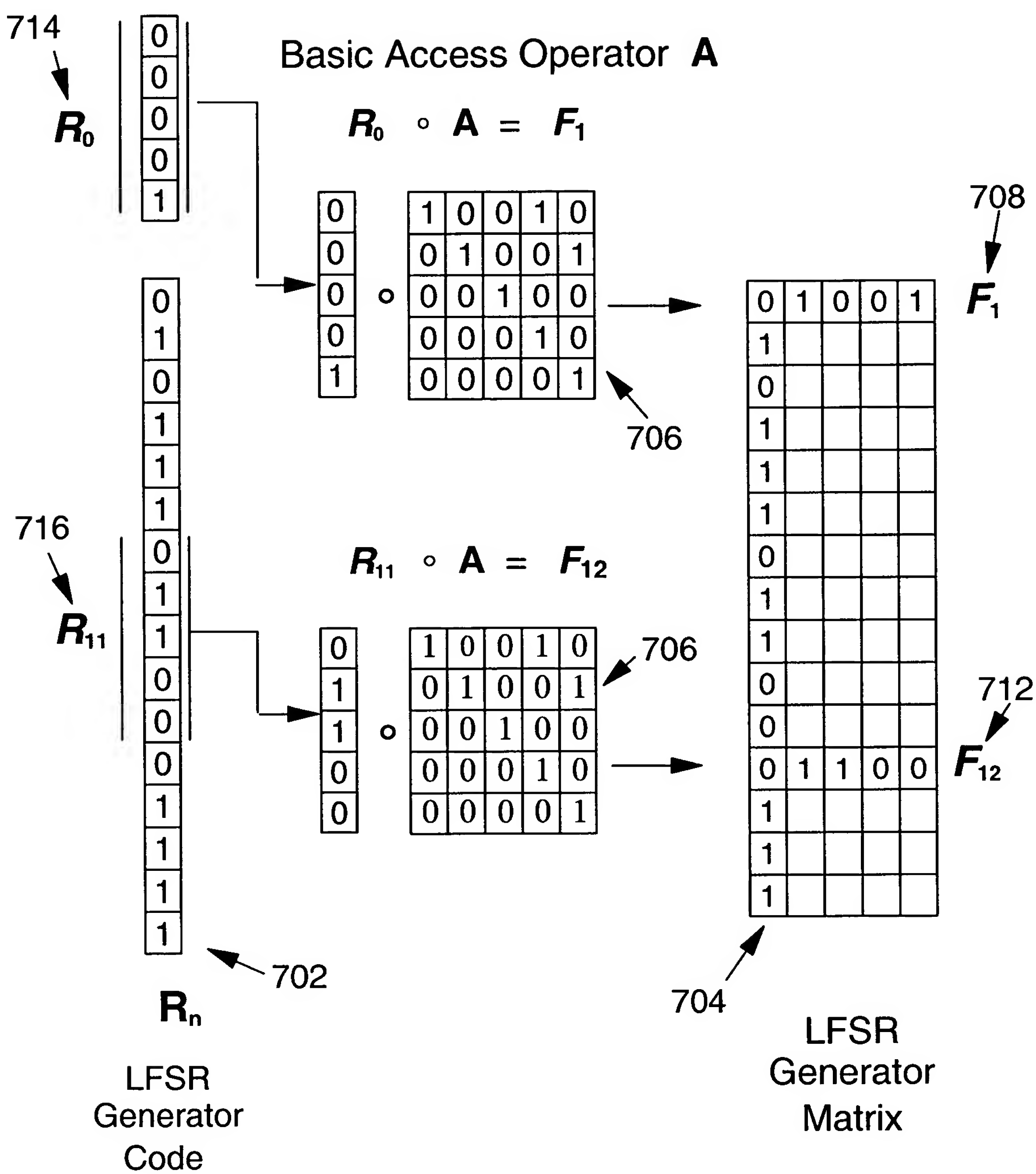
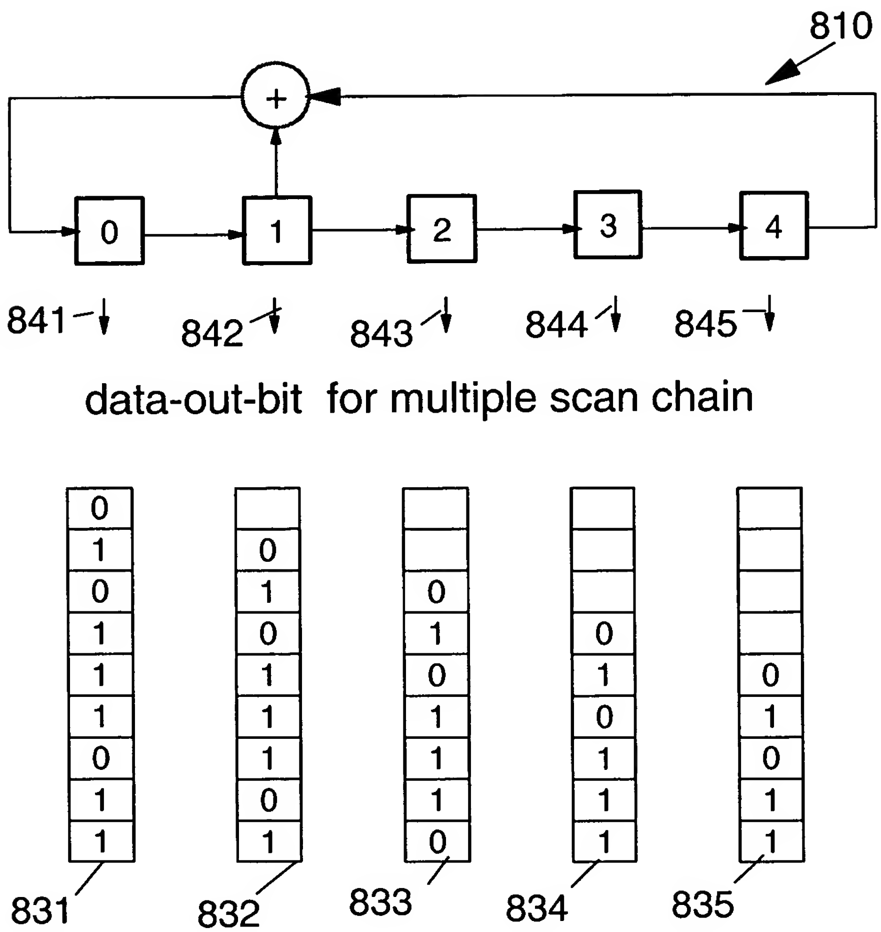

714
R_0
Basic Access Operator A
$R_0 \circ A = F_1$
708
F_1
706
716
R_{11}
$R_{11} \circ A = F_{12}$
706
712
F_{12}
702
R_n
LFSR Generator Code
704
LFSR Generator Matrix

FIG. 7



BIT-Code representation

850

State Function $(F^x)_n = R_n \circ A^x$

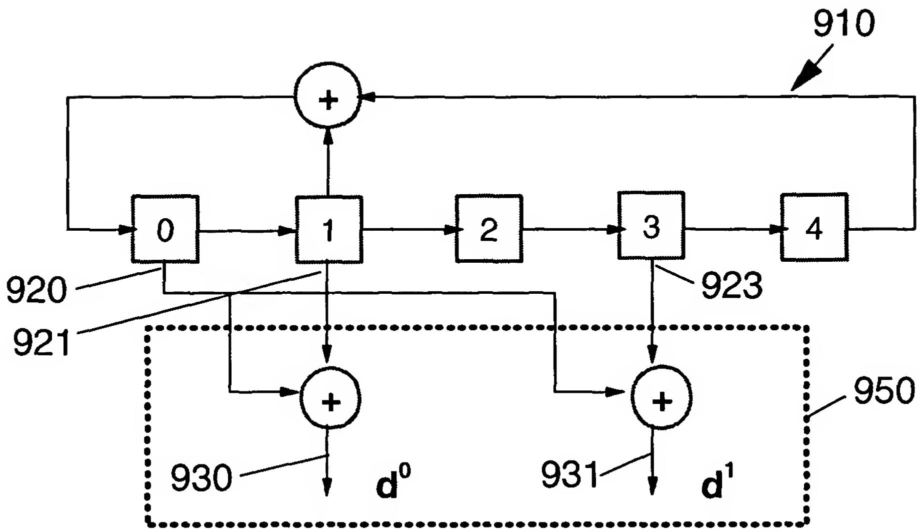
Chain Access Operator $A^x = A \circ P^x$

A Basic Access Operator

$\mathbf{P}^x$ Shift Operator for chain $x = 0, 1, 2, 3, 4$

$\mathbf{R}_n$ LFSR Generator Code $n = 0, 1, 2, \ldots$ cycles

FIG. 8



Spreader XOR-Network
for multiple scan chain

BIT-Code representation

940

State Function $(F^{xy})_n = R_n \circ A^{xy}$

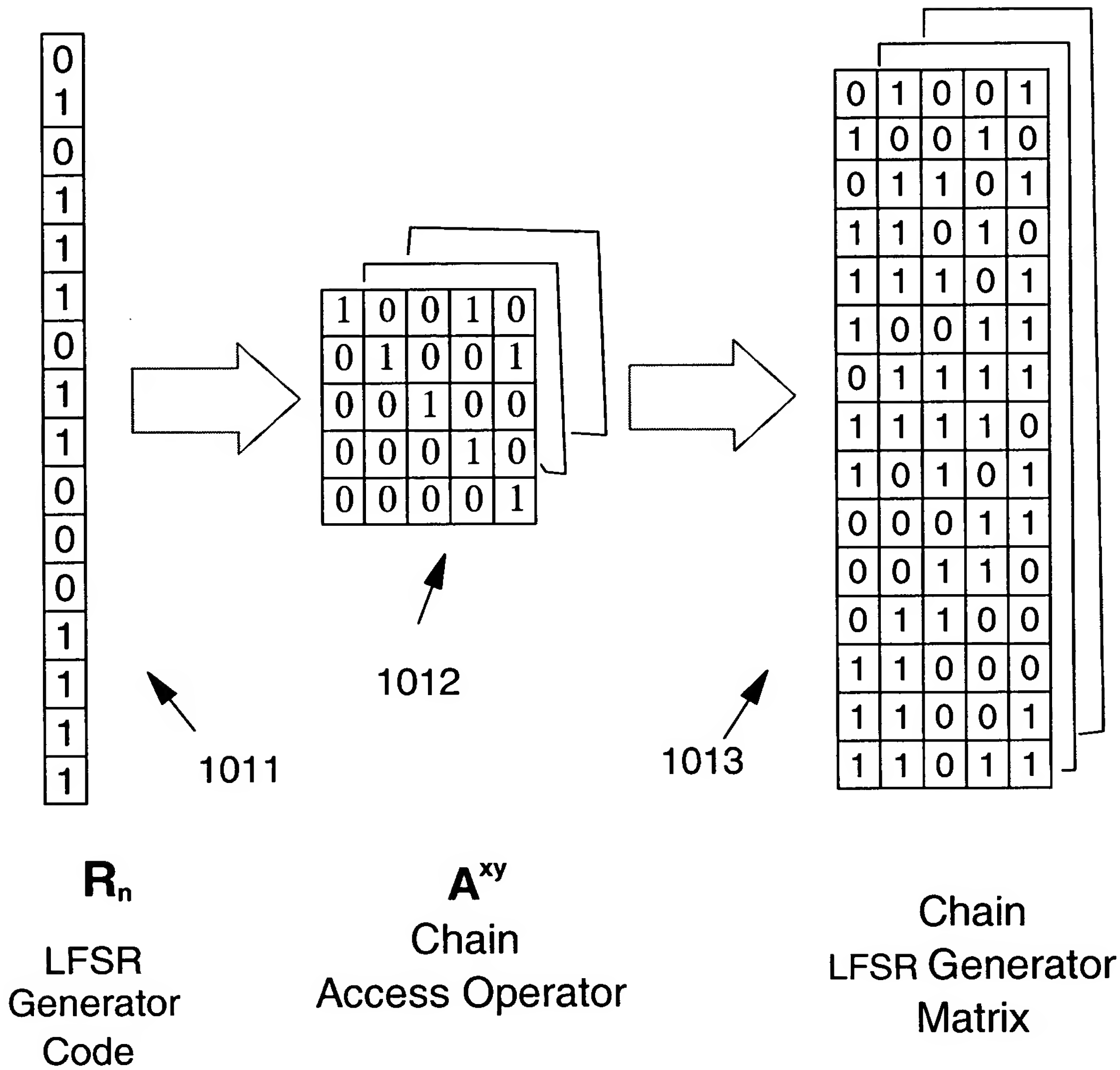
Chain Access Operator $A^{xy} = A \circ (P^x + P^y)$

A Basic Access Operator

$\mathbf{P^x}$ Shift Operator for access $x = 0, 1, 2, 3, 4$

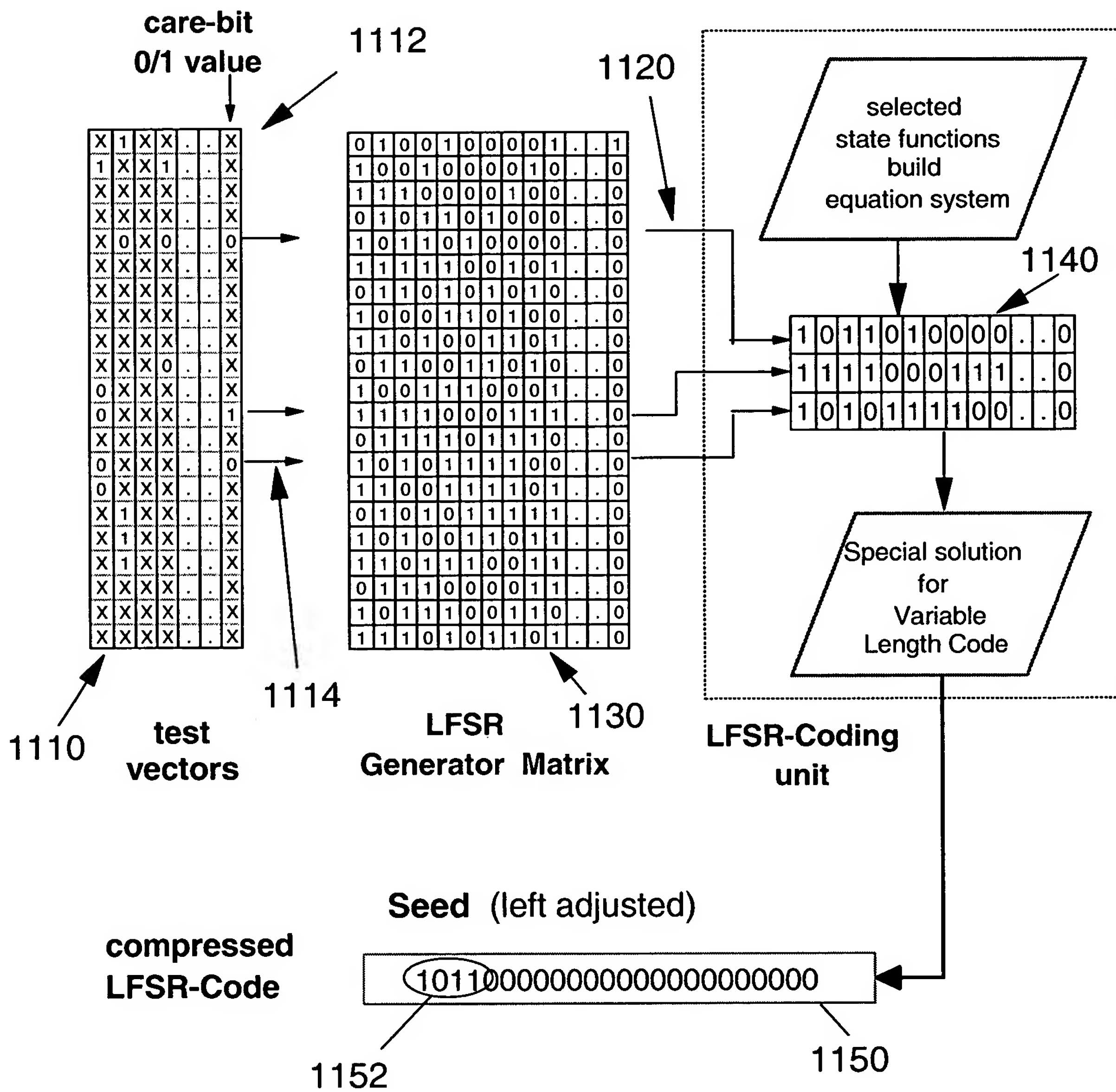
$\mathbf{R_n}$ LFSR Generator Code $n = 0, 1, 2, \ldots$ cycles

FIG. 9



1011
1012
1013
R_n
LFSR
Generator
Code
A^{xy}
Chain
Access Operator
Chain
LFSR Generator
Matrix

FIG. 10



care-bit
0/1 value
1112
1120
selected
state functions
build
equation system
1140
Special solution
for
Variable
Length Code
1110
test
vectors
1114
LFSR
Generator Matrix
1130
LFSR-Coding
unit
Seed (left adjusted)
compressed
LFSR-Code
10110000000000000000000000
1152
1150

FIG. 11